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to the PowerPCTM microprocessors Full chip false timing path identification: applications

Jing Zeng Abadir, M.S. Bhadra, J. Abraham, J.A.

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ASP Somerset Design Center, Motorola Inc., Austin, TX;

This paper appears in: Design, Automation and Test in Europe, 2001.

Conference and Exhibition 2001. Proceedings

03/13/2001 -03/16/2001, 2001 Location: Munich, Germany

Conference ProceedingsStandards

On page(s): 514-518

<u>2001</u>

References Cited: 11

Number of Pages: xxxvi+829

INSPEC Accession Number: 6964654

Abstract:

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<u>analyzed in our initial results. In this paper, we will fully analyze all the timing</u> paths, in many cases only sections of some of the paths in the full-chip were <u>be sensitized. This leads to a pessimistic estimation of the processor speed. Also, </u> <u>have been met. Unfortunately, not all the paths identified using such analysis can</u> speed/performance microprocessors to determine whether timing requirements Static timing anaylsis sets the industry standard in the design methodology of high paths using the ATPG techniques, thus overcoming the gap between the testing bused and the test view on which the ATPG techniques are applied to identify false between the physical design on which the static timing analysis of the chip is ATPG techniques can be used to identify false paths efficiently. Due to the gap <u>timing performance of the chip. In the past we demonstrated initial results of how</u> <u>no amount of engineering effort spent on optimizing such paths can improve the</u>

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Ernst, R.

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<u>Inst. fur Datenverarbeitungsanlagen, Tech. Univ. Braunschweig;</u>

This paper appears in: System Synthesis, 2000. Proceedings. The 13th

<u>International Symposium on</u>

09/20/2000 -09/22/2000,

On page(s): 130-135 ocation: Madrid , Spain

2000

References Cited: 14

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IEEE Catalog Number: 00TH8500

<u>lumber of Pages: xiii+232</u>

NSPEC Accession Number: 6748726

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demonstrates significant improvements in analysis precision data-dependent. A formal analysis of such dependencies leads to intervals rather <u>paths and states of processes, as well as on the target architecture. This paper</u> <u>by taking the execution context into account. The example of an ATM cell handler</u> than single values. These intervals depend on the program properties, execution The timing and power consumption of embedded systems are state and input mproves on previous work by exploiting program segments with single paths and resents an approach to the analysis of process behaviour using intervals. It

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use in timing analysis Primitive path delay faults: identification and their

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Sivaraman, M. Strojwas, A.J.

<u>Carnegie Mellon Univ., Pittsburgh, PA</u>

This paper appears in: Computer-Aided Design of Integrated Circuits and

Systems, IEEE Transactions on

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On page(s): 1347-1362

Volume: 19, Issue: 11,

ISSN: 0278-0070

References Cited: 38

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assumption. From this result, we devise a method to perform timing analysis equal to the maximum circuit delay found under the floating mode of operation primitive PDFs determine the stabilization time of the circuit outputs, based on tight timing constraints, numerous false paths, and large variations in component Present-day digital systems are characterized by large complexity, operation under <u>computation. Our timing analysis approach provides several advantages over</u> <u>multilevel logic circuit. We prove that the maximum primitive PDF delay is exactly</u> which we develop a feasible method to identify the primitive PDFs in a general <u>of these circuits, both before and after fabrication. For combinational circuits, it</u> <u>delays. In such a scenario, it is very important to ensure correct temporal behavio</u> <u>path delay faults (PDFs) are fault-free to ensure that the circuit operates correctly</u> <u>pased on primitive PDF identification which delinks functional analysis from delay</u> or some timing constraint T and all larger timing constraints. We show that <u>ias been shown that it is necessary and sufficient to guarantee that the primitive</u>

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critical paths using ATPG techniques: an experiment A quick and inexpensive method to identify false with a PowerPCTM microprocessor

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Bhadra, J. Abadir, M.S. Abraham, J.A.

Texas Univ., Austin, TX;

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This paper appears in: Custom Integrated Circuits Conference, 2000. CICC.

Proceedings of the IEEE 2000 05/21/2000 -05/24/2000, 2000

Location: Orlando, FL, USA

On page(s): 71-74

2000

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<u>are reported by the static timing analysis tool as potential critical paths, whereas</u> would sensitize that path. This gives rise to the possibility of having paths which circuits to determine whether timing requirements are met. Timing analysis tools Static timing analysis tools are used by designers of high speed/high performance so that the efforts needed to redesign and/or optimize critical paths can be <u>there exists no vector sequence which can sensitize them. Our goal is to identify</u> <u>can report critical paths which are characterized by a transition on each node along</u> these "false critical timing paths" safely and without much overhead the path, however, they cannot generate a "witness" vector which educed. We have devised a simple technique using a tool that we have written

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state of the art fourth generation MPC7400 PowerPCTM microprocessor designed at show the effectiveness of the technique. The salient features of the technique are and a commercial ATPG tool to meet this goal. We applied the technique on the Motorola's PowerPC Design Center in Austin, TX. Our initial experimental results that it is both quick and inexpensive

Index Terms:

automatic test pattern generation integrated circuit testing logic testing microprocessor critical paths identification chips timing ATPG techniques MPC7400 Motorola PowerPC microprocessor false

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Somerset Design Center, Motorola Inc., Austin, TX;

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IEEE Catalog Number: 00TH8528

Number of Pages: xv+836

INSPEC Accession Number: 6852719

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analysis of the chip is based and the test view on which the ATPG technique is applied to eliminate false paths, in many cases only sections of some of the paths <u>efficiently. Due to the gap between the physical design on which the static timing</u> estimation of processor speed, and the engineering efforts spent optimizing such gage the speed of high performance microprocessors. Unfortunately, not all the Static timing analysis sets the industry standard in the design methodology to PowerPCTM <u>paths can not improve the performance of the chip. In the past, we demonstrated</u> <u>paths identified using such analysis can be sensitized. This leads to a pessimistic</u> esting and timing analysis techniques. We applied our method on the second G4 n the full-chip were analyzed in our initial results. In this paper, we fully analyze nitial results of how ATPG technique can be used to eliminate false paths Il the timing paths using the ATPG technique overcoming the gap between the

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